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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/091,003 | ARAI, YOSHIHISA | |
| | Examiner | Art Unit | |
| | David G. Cervetti | 2136 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *06 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-76* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 March 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/6/02,1/30/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 23 (page 33, line11). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**3. Claims 1 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanagawa (US Patent Number: 5,117,380).**

Regarding claim 1, Tanagawa teaches a random number's seed generating circuit comprising (figure 1): an oscillator which generates a clock (column 2, lines 20-

55); and a counter which operates in synchronism with the clock (column 2, lines 29-55), wherein a count value of said counter is output in response to a signal asynchronous with the clock (column 2, lines 20-50, column 3, 1-45), and the output count value is used as an initial value to generate a random number. Tanagawa does not expressly disclose the output count value is used as an initial value to generate a random number, but he teaches that the counters do not necessarily have to be initialized to zero, thus having unpredictable values at power up (column 3, lines 45-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the output count value as an initial value to generate a random number. One of ordinary skill in the art would have been motivated to do so because it was well known in the art to use a count value as an initial or seed value to generate a random number.

Regarding claim 13, Tanagawa teaches a random number's seed generating circuit comprising (figure 1): an oscillator which generates a clock (column 2, lines 20-55); and a counter which operates in synchronism with the clock (column 2, lines 29-55), wherein a timing at which a count value of said counter is output changes at random within a predetermined range in response to a signal (column 2, lines 20-50, column 3, 1-45), and the output count value is used as an initial value to generate a random number. Tanagawa does not expressly disclose the output count value is used as an initial value to generate a random number, but he teaches that the counters do not necessarily have to be initialized to zero, thus having unpredictable values at power up (column 3, lines 45-65). Therefore, it would have been obvious to one having

ordinary skill in the art at the time the invention was made to use the output count value as an initial value to generate a random number. One of ordinary skill in the art would have been motivated to do so because it was well known in the art to use a count value as an initial or seed value to generate a random number.

**4. Claims 25 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanagawa, and further in view of Domenik et al. (US Patent Number: 4,694,412).**

Regarding claim 25, Tanagawa teaches a random number's seed generating circuit having an oscillator which generates a clock and a counter which operates in synchronism with the clock (figure 1, column 2, lines 20-50, column 3, 1-45); and a random number generating circuit which generates a random number using an initial value generated by said random number's seed generating circuit, wherein a count value of said counter is output in response to a signal asynchronous with the clock (column 2, lines 20-50), the output count value is used as the initial value, and transfer data is kept secret using the random number. Tanagawa does not expressly disclose the output count value is used as the initial value. Tanagawa teaches that the counters do not necessarily have to be initialized to zero, thus having unpredictable values at power up (column 3, lines 45-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the output count value as an initial value to generate a random number. One of ordinary skill in the art would have been motivated to do so because it was well known in the art to use a count value as an initial value to generate a random number. Tanagawa does not expressly disclose

that transfer data is kept secret using the random number. However, Domenik et al. teach encrypting data using the random number (column 3, lines 1-52). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to keep transfer data secret using the random number. One of ordinary skill in the art would have been motivated to do so because it was well known in the art at the time the invention was made to protect transfer data using a random number.

Regarding claim 38, Tanagawa teaches a random number's seed generating circuit having an oscillator which generates a clock and a counter which operates in synchronism with the clock (column 2, lines 20-50, column 3, 1-45); and a random number generating circuit which generates a random number using an initial value generated by said random number's seed generating circuit, wherein a timing at which a count value of said counter is output changes at random within a predetermined range in response to a signal (column 2, lines 20-50, column 3, 1-45), the output count value is used as the initial value, and transfer data is kept secret using the random number. Tanagawa does not expressly disclose the output count value is used as the initial value and that transfer data is kept secret using the random number. Tanagawa teaches that the counters do not necessarily have to be initialized to zero, thus having unpredictable values at power up (column 3, lines 45-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the output count value as an initial value to generate a random number. One of ordinary skill in the art would have been motivated to do so because it was well known in the art to use a count value as an initial value to generate a random number. However, Domenik et al.

teach encrypting data using the random number (column 3, lines 1-52). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to keep transfer data secret using the random number. One of ordinary skill in the art would have been motivated to do so because it was well known in the art at the time the invention was made to protect transfer data using a random number.

**5. Claims 51 and 64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanagawa, and further in view of Maeda et al. (US Patent Number: 6,611,907) and Domenik et al.**

Regarding claim 51, Tanagawa teaches a random number's seed generating circuit having an oscillator which generates a clock (column 2, lines 20-50, column 3, 1-45) and a counter which operates in synchronism with the clock (column 2, lines 20-50, column 3, 1-45), and a random number generating circuit which generates a random number using an initial value generated by said random number's seed generating circuit (column 2, lines 20-50, column 3, 1-45). Tanagawa does not expressly disclose using the random number generator in a SD memory card driven by a driver and having a data protecting function, wherein a count value of said counter is output in response to a signal asynchronous with the clock, the output count value is used as the initial value, and transfer data is kept secret using the random number. Tanagawa teaches that the counters do not necessarily have to be initialized to zero, thus having unpredictable values at power up (column 3, lines 45-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to output in response to a signal asynchronous with the clock the count value of said counter, and

use the output count value as an initial value to generate a random number. One of ordinary skill in the art would have been motivated to do so because it was well known in the art to use a count value as an initial or seed value to generate a random number. Tanagawa does not expressly disclose that transfer data is kept secret using the random number. However, Domenik et al. teach encrypting data using the random number (column 3, lines 1-52). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to keep transfer data secret using the random number. One of ordinary skill in the art would have been motivated to do so because it was well known in the art at the time the invention was made to protect transfer data using a random number. Maeda et al. teach a random number generated by a SD memory card (figures 2A, 2B, 2C, 3A). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the system of Tanagawa with the memory card of Maeda et al. One of ordinary skill in the art would have been motivated to do so because it was well known in the art to use random number generator circuits within memory cards.

Regarding claim 64, Tanagawa teaches a random number's seed generating circuit having an oscillator which generates a clock (column 2, lines 20-50, column 3, 1-45) and a counter which operates in synchronism with the clock (column 2, lines 20-50, column 3, 1-45), and a random number generating circuit which generates a random number using an initial value generated by said random number's seed generating circuit (column 2, lines 20-50, column 3, 1-45). Tanagawa does not expressly disclose using the random number generator in a SD memory card driven by a driver and having

a data protecting function, wherein a timing at which a count value of said counter is output changes at random within a predetermined range in response to a signal, the output count value is used as the initial value, and transfer data is kept secret using the random number. Tanagawa teaches that the counters do not necessarily have to be initialized to zero, thus having unpredictable values at power up (column 3, lines 45-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to output in response to a signal asynchronous with the clock the count value of said counter, and use the output count value as an initial value to generate a random number. One of ordinary skill in the art would have been motivated to do so because it was well known in the art to use a count value as an initial value to generate a random number. Tanagawa does not expressly disclose that transfer data is kept secret using the random number. However, Domenik et al. teach encrypting data using the random number (column 3, lines 1-52). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to keep transfer data secret using the random number. One of ordinary skill in the art would have been motivated to do so because it was well known in the art at the time the invention was made to protect transfer data using a random number. Maeda et al. teach a random number generated by a SD memory card (figures 2A, 2B, 2C, 3A). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the system of Tanagawa with the memory card of Maeda et al. One of ordinary skill in the art would have been motivated to do so because it was well known in the art to use random number generator circuits within memory cards.

**6. Claims 2-5, 10, 12, 14-17, 22, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanagawa.**

Regarding claims 2 and 14, Tanagawa teaches wherein the signal is a signal output from a power-on reset circuit upon detecting that a power supply is turned on, and a power supply potential is stabilized (column 2, lines 40-67, column 3, lines 1-45).

Regarding claims 3 and 15, Tanagawa teaches wherein the signal is an operation start signal output from a controller (column 2, lines 9-20).

Regarding claims 4 and 16, Tanagawa teaches wherein the operation start signal is output when the controller recognizes that a power supply is turned on (column 2, lines 50-67).

Regarding claims 5 and 17, Tanagawa does not disclose expressly wherein the operation start signal is output when the controller recognizes that a predetermined operation is performed by a user. However, Examiner takes Official Notice that performing an operation triggered by a user is conventional and well known. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to output a signal when a user performs an operation since Examiner takes Official Notice that it was conventional and well known.

Regarding claims 10 and 22, Tanagawa teaches wherein a timing at which the count value is output changes within a range of time longer than a period of the clock every time the count value is output (column 3, lines 25-40).

Regarding claims 12 and 24, Tanagawa teaches wherein when a random number generating circuit to which the signal is input is set in an operative state, the

count value is simultaneously received by the random number generating circuit as the initial value (column 2, lines 40-67, column 3, lines 1-45).

**7. Claims 6, 11, 18, 23, 26-31, 35-37, 39-44, and 48-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanagawa, and further in view of Domenik et al.**

Regarding claims 6 and 18, Tanagawa does not disclose expressly wherein said oscillator is set in an inoperative state or lowers a frequency of the clock after the count value is output in response to the signal. Tanagawa teaches that the output occurs only when a high read signal is received (column 2, lines 40-54). However, Domenik et al. teach wherein said oscillator is set in an inoperative state or lowers a frequency of the clock after the count value is output in response to the signal (column 9, lines 30-67). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to set the oscillator in an inoperative state or lower a frequency of the clock after the count value is output in response to the signal. One of ordinary skill in the art would have been motivated to do so because stopping processing after a result is output was well known in the art.

Regarding claims 11 and 23, Tanagawa does not disclose expressly comprising a latch circuit which latches the count value on the basis of the signal, wherein the count value latched by said latch circuit is used as the initial value. However, Domenik et al. teach using a latch circuit (column 6, lines 1-30). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to set the oscillator in an inoperative state or lower a frequency of the clock after the count value

is output in response to the signal. One of ordinary skill in the art would have been motivated to do so because using a count value as initial or seed value for a random number generator was well known in the art.

Regarding claims 26 and 39, the combination of Tanagawa and Domenik et al. teaches the limitations as set forth under claims 25 and 38 respectively above. Furthermore, Tanagawa teaches wherein the random number is generated every time a power supply is turned on, every time the data is written or read, or every time a predetermined operation is performed by a user (column 2, lines 40-67, column 3, lines 1-45).

Regarding claims 27 and 40, the combination of Tanagawa and Domenik et al. teaches the limitations as set forth under claims 25 and 38 respectively above. Furthermore, Tanagawa teaches wherein the signal is a signal output from a power-on reset circuit upon detecting that a power supply is turned on, and a power supply potential is stabilized (column 2, lines 40-67, column 3, lines 1-45).

Regarding claims 28 and 41, the combination of Tanagawa and Domenik et al. teaches the limitations as set forth under claims 25 and 38 respectively above. Furthermore, Tanagawa teaches wherein the signal is an operation start signal output from a controller (column 2, lines 9-20).

Regarding claims 29 and 42, the combination of Tanagawa and Domenik et al. teaches the limitations as set forth under claims 28 and 41 respectively above. Furthermore, Tanagawa teaches wherein the operation start signal is output when the controller recognizes that a power supply is turned on (column 2, lines 50-67).

Regarding claims 30 and 43, the combination of Tanagawa and Domenik et al. does not disclose expressly wherein the operation start signal is output when the controller recognizes that a predetermined operation is performed by a user. However, Examiner takes Official Notice that performing an operation triggered by a user is conventional and well known. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to output a signal when a user performs an operation since Examiner takes Official Notice that it was conventional and well known.

Regarding claims 31 and 44, the combination of Tanagawa and Domenik et al. teaches the limitations as set forth under claims 25 and 38 respectively above. Furthermore, Domenik et al. teach wherein said oscillator is set in an inoperative state or lowers a frequency of the clock after the count value is output in response to the signal (column 9, lines 30-67). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to set the oscillator in an inoperative state or lower a frequency of the clock after the count value is output in response to the signal. One of ordinary skill in the art would have been motivated to do so because stopping processing after a result is output was well known in the art.

Regarding claims 35 and 48, the combination of Tanagawa and Domenik et al. teaches the limitations as set forth under claims 25 and 38 respectively above. Furthermore, Tanagawa teaches wherein a timing at which the count value is output changes within a range of time longer than a period of the clock every time the count value is output (column 3, lines 25-40).

Regarding claims 36 and 49, the combination of Tanagawa and Domenik et al. teaches the limitations as set forth under claims 25 and 38 respectively above. Furthermore, Domenik et al. teach using a latch circuit (column 6, lines 1-30). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to set the oscillator in an inoperative state or lower a frequency of the clock after the count value is output in response to the signal. One of ordinary skill in the art would have been motivated to do so because using a count value as initial or seed value for a random number generator was well known in the art.

Regarding claims 37 and 50, the combination of Tanagawa and Domenik et al. teaches the limitations as set forth under claims 25 and 38 respectively above. Furthermore, Tanagawa teaches wherein when a random number generating circuit to which the signal is input is set in an operative state, the count value is simultaneously received by the random number generating circuit as the initial value (column 2, lines 40-67, column 3, lines 1-45).

**8. Claims 7-9 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanagawa, and further in view of Hoffman (US Patent Number: 5,706,218).**

Regarding claims 7 and 19, Tanagawa does not disclose expressly wherein said oscillator is a voltage-controlled oscillator having an external terminal, said oscillator and external terminal are electrically disconnected before the count value is output, and said oscillator and external terminal are electrically connected after the count value is output. However, Hoffman teaches wherein said oscillator is a voltage-controlled

oscillator having an external terminal, said oscillator and external terminal are electrically disconnected before the count value is output, and said oscillator and external terminal are electrically connected after the count value is output (columns 1-4, figures 1, 3). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a voltage-controlled oscillator wherein said oscillator and external terminal are electrically disconnected before the count value is output, and said oscillator and external terminal are electrically connected after the count value is output. One of ordinary skill in the art would have been motivated to do so because the use of voltage-controlled oscillators with random number generators was well known in the art.

Regarding claims 8 and 20, the combination of Tanagawa and Hoffman teaches the limitations as set forth under claims 7 and 19, respectively above. Furthermore, Hoffman teaches wherein a switch circuit controlled by the signal is connected between said oscillator and the external terminal (columns 1-4, figures 1, 3).

Regarding claims 9 and 21, the combination of Tanagawa and Hoffman does not disclose expressly wherein after the count value is output, the clock is used as a system clock. However, Tanagawa teaches the clock being independent from the system clock (column 2, lines 9-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the clock as a system clock after the count value was output. One of ordinary skill in the art would have been motivated to do so because the use of system clocks was well known in the art.

**9. Claims 32-34 and 45-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanagawa and Domenik et al., and further in view of Hoffman.**

Regarding claims 32 and 45, the combination of Tanagawa and Domenik et al. does not disclose expressly wherein said oscillator is a voltage-controlled oscillator having an external terminal, said oscillator and external terminal are electrically disconnected before the count value is output, and said oscillator and external terminal are electrically connected after the count value is output. However, Hoffman teaches wherein said oscillator is a voltage-controlled oscillator having an external terminal, said oscillator and external terminal are electrically disconnected before the count value is output, and said oscillator and external terminal are electrically connected after the count value is output (columns 1-4, figures 1, 3). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a voltage-controlled oscillator wherein said oscillator and external terminal are electrically disconnected before the count value is output, and said oscillator and external terminal are electrically connected after the count value is output. One of ordinary skill in the art would have been motivated to do so because the use of voltage-controlled oscillators with random number generators was well known in the art.

Regarding claims 33 and 46, the combination of Tanagawa, Domenik et al., and Hoffman teaches the limitations as set forth under claims 32 and 45, respectively above. Furthermore, Hoffman teaches wherein a switch circuit controlled by the signal is connected between said oscillator and the external terminal (columns 1-4, figures 1, 3).

Regarding claims 34 and 47, the combination of Tanagawa, Domenik et al., and Hoffman does not disclose expressly wherein after the count value is output, the clock is used as a system clock. However, Tanagawa teaches the clock being independent from the system clock (column 2, lines 9-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the clock as a system clock after the count value was output. One of ordinary skill in the art would have been motivated to do so because the use of system clocks was well known in the art.

**10. Claims 52-57, 61-63, 65-70, and 74-76 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanagawa, and further in view of Maeda et al. and Domenik et al.**

Regarding claims 52 and 65, the combination of Tanagawa, Maeda et al., and Domenik et al. teaches the limitations as set forth under claims 51 and 64 respectively above. Furthermore, Tanagawa teaches wherein the random number is generated every time a power supply is turned on, every time the data is written or read, or every time a predetermined operation is performed by a user (column 2, lines 40-67, column 3, lines 1-45).

Regarding claims 53 and 66, the combination of Tanagawa, Maeda et al., and Domenik et al. teaches the limitations as set forth under claims 51 and 64 respectively above. Furthermore, Tanagawa teaches wherein the signal is a signal output from a power-on reset circuit upon detecting that a power supply is turned on, and a power supply potential is stabilized (column 2, lines 40-67, column 3, lines 1-45).

Regarding claims 54 and 67, the combination of Tanagawa, Maeda et al., and Domenik et al. teaches the limitations as set forth under claims 51 and 64 respectively above. Furthermore, Tanagawa teaches wherein the signal is an operation start signal output from a controller (column 2, lines 9-20).

Regarding claims 55 and 68, the combination of Tanagawa, Maeda et al., and Domenik et al. teaches the limitations as set forth under claims 54 and 67 respectively above. Furthermore, Tanagawa teaches wherein the operation start signal is output when the controller recognizes that a power supply is turned on (column 2, lines 50-67).

Regarding claims 56 and 69, the combination of Tanagawa, Maeda et al., and Domenik et al. does not disclose expressly wherein the operation start signal is output when the controller recognizes that a predetermined operation is performed by a user. However, Examiner takes Official Notice that performing an operation triggered by a user is conventional and well known. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to output a signal when a user performs an operation since Examiner takes Official Notice that it was conventional and well known.

Regarding claims 57 and 70, the combination of Tanagawa, Maeda et al., and Domenik et al. does not disclose expressly wherein said oscillator is set in an inoperative state or lowers a frequency of the clock after the count value is output in response to the signal. Tanagawa teaches that the output occurs only when a high read signal is received (column 2, lines 40-54). Furthermore, Domenik et al. teach wherein said oscillator is set in an inoperative state or lowers a frequency of the clock after the

count value is output in response to the signal (column 9, lines 30-67). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to set the oscillator in an inoperative state or lower a frequency of the clock after the count value is output in response to the signal. One of ordinary skill in the art would have been motivated to do so because stopping processing after a result is output was well known in the art.

Regarding claims 61 and 74, the combination of Tanagawa, Maeda et al., and Domenik et al. teaches the limitations as set forth under claims 51 and 64 respectively above. Furthermore, Tanagawa teaches wherein a timing at which the count value is output changes within a range of time longer than a period of the clock every time the count value is output (column 3, lines 25-40).

Regarding claims 62 and 75, the combination of Tanagawa, Maeda et al., and Domenik et al. teaches the limitations as set forth under claims 51 and 64 respectively above. Furthermore, Domenik et al. teach using a latch circuit (column 6, lines 1-30). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to set the oscillator in an inoperative state or lower a frequency of the clock after the count value is output in response to the signal. One of ordinary skill in the art would have been motivated to do so because using a count value as initial value for a random number generator was well known in the art.

Regarding claims 63 and 76, the combination of Tanagawa, Maeda et al., and Domenik et al. teaches the limitations as set forth under claims 51 and 64 respectively above. Furthermore, Tanagawa teaches wherein when a random number generating

circuit to which the signal is input is set in an operative state, the count value is simultaneously received by the random number generating circuit as the initial value (column 2, lines 40-67, column 3, lines 1-45).

**11. Claims 58-60 and 71-73 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanagawa, Maeda et al., and Domenik et al., and further in view of Hoffman.**

Regarding claims 58 and 71, the combination of Tanagawa, Maeda et al., and Domenik et al. does not disclose expressly wherein said oscillator is a voltage-controlled oscillator having an external terminal, said oscillator and external terminal are electrically disconnected before the count value is output, and said oscillator and external terminal are electrically connected after the count value is output. However, Hoffman teaches wherein said oscillator is a voltage-controlled oscillator having an external terminal, said oscillator and external terminal are electrically disconnected before the count value is output, and said oscillator and external terminal are electrically connected after the count value is output (columns 1-4, figures 1, 3). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a voltage-controlled oscillator wherein said oscillator and external terminal are electrically disconnected before the count value is output, and said oscillator and external terminal are electrically connected after the count value is output. One of ordinary skill in the art would have been motivated to do so because the use of voltage-controlled oscillators with random number generators was well known in the art.

Regarding claims 59 and 72, the combination of Tanagawa, Maeda et al., Domenik et al., and Hoffman teaches the limitations as set forth under claims 58 and 71, respectively above. Furthermore, Hoffman teaches wherein a switch circuit controlled by the signal is connected between said oscillator and the external terminal (columns 1-4, figures 1, 3).

Regarding claims 60 and 73, the combination of Tanagawa, Maeda et al., Domenik et al., and Hoffman does not disclose expressly wherein after the count value is output, the clock is used as a system clock. However, Tanagawa teaches the clock being independent from the system clock (column 2, lines 9-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the clock as a system clock after the count value was output. One of ordinary skill in the art would have been motivated to do so because the use of system clocks was well known in the art.

***Conclusion***

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David G. Cervetti whose telephone number is (571) 272-5861. The examiner can normally be reached on Monday-Friday 7:00 am - 5:00 pm, off on Wednesday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz R. Sheikh can be reached on (571) 272-3795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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